Aatish Varma

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EDUCATION

New York University – College of Arts and Sciences *September 2016 – May 2020*
Bachelor of Arts - Computer Science, Minor in Mathematics Cumulative GPA - 3.73/4.0
Honors: Latin Honors – Cum Laude, University Honors Scholar Major GPA - 3.81/4.0

SKILLS

Programming:
Python, Java, JavaScript (Node, React), Rust (Proficient)
SQL, Go (Adequate)

Technologies:
AWS (EC2, Timeseries)
PostgreSQL

EXPERIENCE

Research Assistant - NYU Systems and Networking Lab *October 2018 – May 2020*
Supervisor: Professor Anirudh Sivaraman, Ph.D.

- Worked on multiple projects (see **Chipmunk** and **Druzhba** below) at the intersection of Program Synthesis, Computer Networks, and Computer Architecture
- Published three papers in top conferences (ACM SIGCOMM, ACM HotNets)

Software Engineering Intern - General Electric (GE) - Digital *May 2018 – August 2018*

- Added audit functionality to the Time Series Go Pipeline to monitor processes using the Predix SDK
- Implemented an Amazon S3 Wrapper Interface for Asynchronous Query Storage in Java
- Queried 500,000 data points from multiple PostgreSQL databases and generated data visualizations

RESEARCH PROJECTS

Chipmunk: Synthesis-Aided compiler for Programmable Switches
Technologies Used: **Python, C++, Z3, Sketch, ANTLR**

- Co-wrote a compiler in Python which compiles C-like code to a programmable switch using program synthesis
- Created a Domain Specific Language (DSL) used to specify a router's pipeline specification and generate hardware code
- Implemented a splicing algorithm which heuristically split a program into smaller sub-programs which could be run in parallel, yielding a 4x speed up in compilation time

Druzhba: Network Switch Hardware Simulator
Technologies Used: **Rust, LALRPOP (Rust Parser Generator), RISC-V**

- Developed a hardware simulator in Rust to allow network operators to test data plane programs before permanently setting their hardware configurations
- Modeled low level hardware primitives in software using RISC-V
- Implemented Compiler Optimizations such as Constant Folding to speed-up runtime by 2.5x

PUBLICATIONS

- **Testing Compilers for Programmable Switches Through Switch Hardware Simulation**
  Michael Dean Wong, **Aatish Varma**, Anirudh Sivaraman
  ACM CAL 2020 (In Submission)
- **Switch Code Generation using Program Synthesis**
  Xiangyu Gao, Taegyun Kim, Michael Dean Wong, Divya Raghunathan, **Aatish Varma**, Pravein Govind Kannan, Anirudh Sivaraman, Srinivas Narayana, Aarti Gupta
  ACM SIGCOMM 2020
- **Autogenerating Fast Packet-Processing Code Using Program Synthesis**
  Xiangyu Gao, Taegyun Kim, **Aatish Varma**, Anirudh Sivaraman, and Srinivas Narayana
  ACM HotNets 2019

LEADERSHIP & ACTIVITIES

Head Teaching Assistant - NYU Computer Science Department *September 2019 – December 2019*
Course: Undergraduate Computer Networks, Instructor: Professor Aurojit Panda, Ph.D.

- Taught topics related to BGP, intra-domain routing, and router hardware